CBCS Scheme

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15EE34

Third Semester B.E. Degree Examination, Dec.2016/Jan.2017
Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 80

Note: Answer FIVE full questions, choosing one full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice

Module-1

1 a. Design a collector to base bias circuit for the following specifications : $V_{CC} = 10V$, $V_{CE} = 5V$, $I_C = 1mA$, $\beta = 50$. If β varies from 25 to 75, find the change in collector current. **(07 Marks)**

b. What are the different biasing circuits? Find an expression for stability factor 'S' of each biasing circuit. **(09 Marks)**

OR

2 a. Design a voltage divider biasing circuit with a supply voltage of 10V and $V_{CE} = \frac{V_{CC}}{2}$. The load resistance is 2KΩ. Take $\beta = 100$. **(09 Marks)**

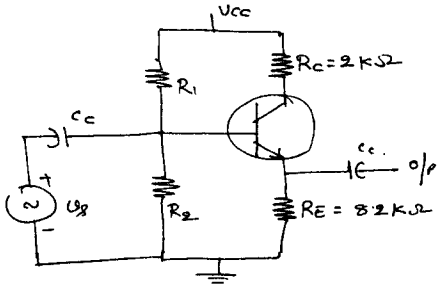
b. Explain the operation of transistor as switch along with suitable circuit and necessary waveforms. Highlight the design procedure. **(07 Marks)**

Module-2

3 a. Draw the circuit of common emitter amplifier with voltage divider biasing. Derive the expression for current gain, voltage gain, input and output impedance using the model. **(08 Marks)**

b. For the following circuit, find current gain, voltage gain, input and output impedance. **(08 Marks)**

Fig.Q3(b)



Vcc = 10V
R1 = 47kΩ
R2 = 56kΩ
RE = 8.2 kΩ
β = 100

OR

4 a. Starting from fundamentals, define h parameters and obtain an h – parameter equivalent circuit of common emitter configuration. **(08 Marks)**

b. Derive suitable expressions to explain the effect of cascading of amplifiers on lower and upper cut off frequencies. **(08 Marks)**

Module-3

5 a. What is a Cascade amplifier? Draw a practical circuit with cascade connection and derive the expressions for current gain, voltage gain, input and output impedance using r_e model. **(10 Marks)**

b. Explain the block diagram of a feedback amplifier. **(06 Marks)**

OR

6 a. Draw the circuit of Darlington emitter follower with voltage divider bias. Calculate input impedance, voltage gain and output impedance. Take $\beta_1 = \beta_2 = 100$. **(08 Marks)**
$R_1 = R_2 = 100K$, $R_E = 5k\Omega$. Take $r_e = 0.1K\Omega$.

b. Draw the block diagram of voltage series feedback amplifier and find the effect of feedback on input and output impedances. **(08 Marks)**

Module-4

7 a. Draw the circuit of class – A transformer coupled power amplifier. Explain the operation of the circuit with the help of neat waveforms. Also derive an expression for maximum efficiency of conversion. **(08 Marks)**

b. Draw the circuit of Wien bridge oscillator and derive an expression for frequency of oscillator. **(08 Marks)**

OR

8 a. Explain the classification of power amplifier with neat circuit diagram and waveforms of collector current and collector voltage for each type of power amplifier. **(10 Marks)**

b. Explain the principle of operation of oscillator and the effect of loop gain ($A\beta$) on the output of oscillator. **(06 Marks)**

Module-5

9 a. With the help of neat diagrams, explain the construction, working and characteristics of n – channel JFET. **(08 Marks)**

b. For the following circuit, find voltage gain and output impedance
i) If $r_d = 20K\Omega$ ii) If $r_d = \infty$. **(08 Marks)**

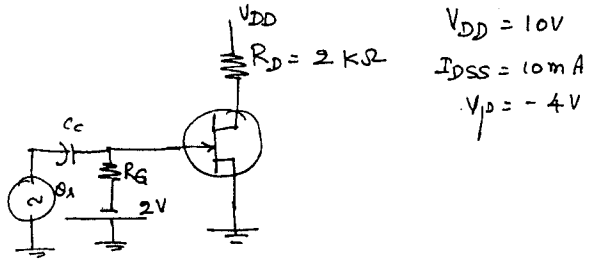


Fig.Q9(b)

OR

10 a. Explain the construction, working and characteristics of n – channel depletion MOSFET. **(08 Marks)**

b. Draw the circuit of common source amplifier using JFET, with the help of small signal model derive an expression for current gain, input impedance, voltage gain and output impedance. **(08 Marks)**

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